PVP 14

Code: IT4T5

II B.Tech II Semester Regular/Supplementary Examinations
April 2019

COMPUTER SYSTEM ARCHITECTURE
(INFORMATION TECHNOLOGY)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11 x 2 = 22 M

1. a) What is a micro operation?
   b) Mention any Three Arithmetic micro-operations.
   c) What is an instruction code?
   d) What is the use of Program Counter?
   e) What is zero address instruction?
   f) What is reverse polish notation?
   g) What is the use of Signed 2's complement representation.
   h) What is the use of Associate Memory?
   i) How to measure the performance of the cache memory?
   j) What is IOP?
   k) What is pipelining?

PART – B

Answer any ***THREE*** questions. All questions carry equal marks.

3 x 16 = 48 M

2. a) Draw and explain 4-bit arithmetic circuit. 8 M

   b) Design a digital circuit that performs the four logic operations of ex-OR, ex-NOR, NOR and NAND using two selection variables. 8 M

3. a) Explain briefly about memory reference instructions. 8 M

   b) Explain about Input-Output Interrupt. 8 M

4. a) Write a program to evaluate the arithmetic statement

   $$X = A - B + C * (D * E - F)$$

   Using a general register computer with three address instructions. 8 M

   b) Explain in detail about the program control instructions. 8 M

5. a) Draw and explain the flow chart for signed magnitude addition and subtraction. 8 M

   b) Discuss various Memory Mapping techniques in Cache memory. 8 M

6. a) Explain about Interrupt-initiated I/O. 8 M

b) What is four segment instruction pipelining? 8 M